



FINALTERM EXAMINATION
SEMESTER FALL 2004
CS302-Digital Logic Design (S1)

Total Marks:70
Duration:120 Min

Student ID / Login ID	
Name	
PVC Name / Code	
Date	

Maximum Time Allowed: (2 Hours)

Please read the following instructions carefully before attempting any of the questions:

1. Attempt all questions.
2. Calculators are **NOT** allowed.
3. Do not ask any questions about the contents of this examination from anyone.
 - a. If you think that there is something wrong with any of the questions, attempt it to the best of your understanding.
 - b. If you believe that some essential piece of information is missing, make an appropriate assumption and use it to solve the problem.
4. **Circuit Diagrams**, **Equations** and **Truth Tables** should be clear.
Write down all the steps in Subjective Questions. Marks will be deducted for missing steps.

****WARNING: Please note that Virtual University takes serious note of unfair means. Anyone found involved in cheating will get an `F` grade in this course.**

For Teacher's use only								
Question	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Total
Marks								

Question No: 1

Marks: 8+8

a) Convert each of the following POS expression to minimum SOP expression using a Karnaugh Map.

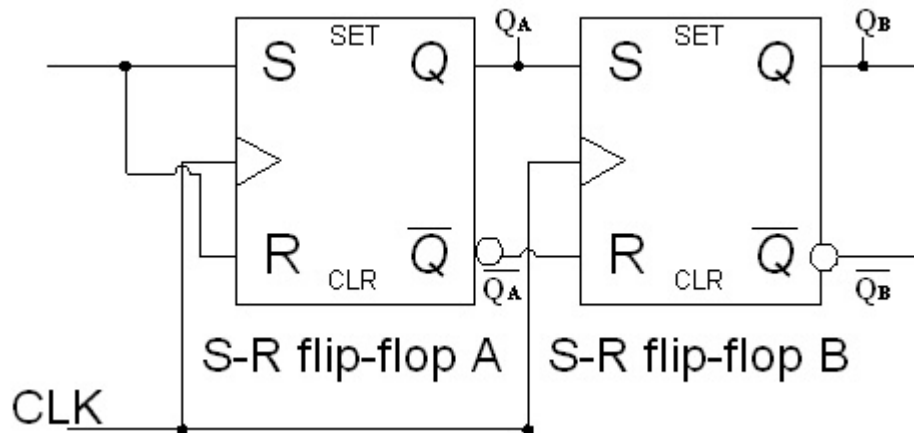
$$(A + B)(\bar{A} + \bar{B} + C)(B + C + D)(A + B + C + D)$$

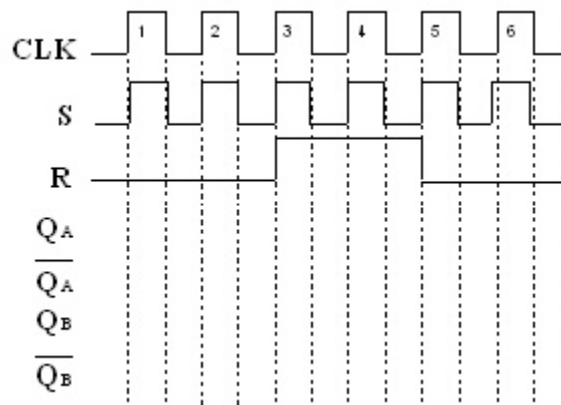
b) Convert the decimal numbers 78 and 34 into Octal. Using octal addition, add the two numbers and convert the octal result back into decimal and verify the answer.

Question No: 2

Marks: 8

Draw the timing diagram of Q_A , \bar{Q}_A , Q_B and \bar{Q}_B . Assume the Positive edge triggering.

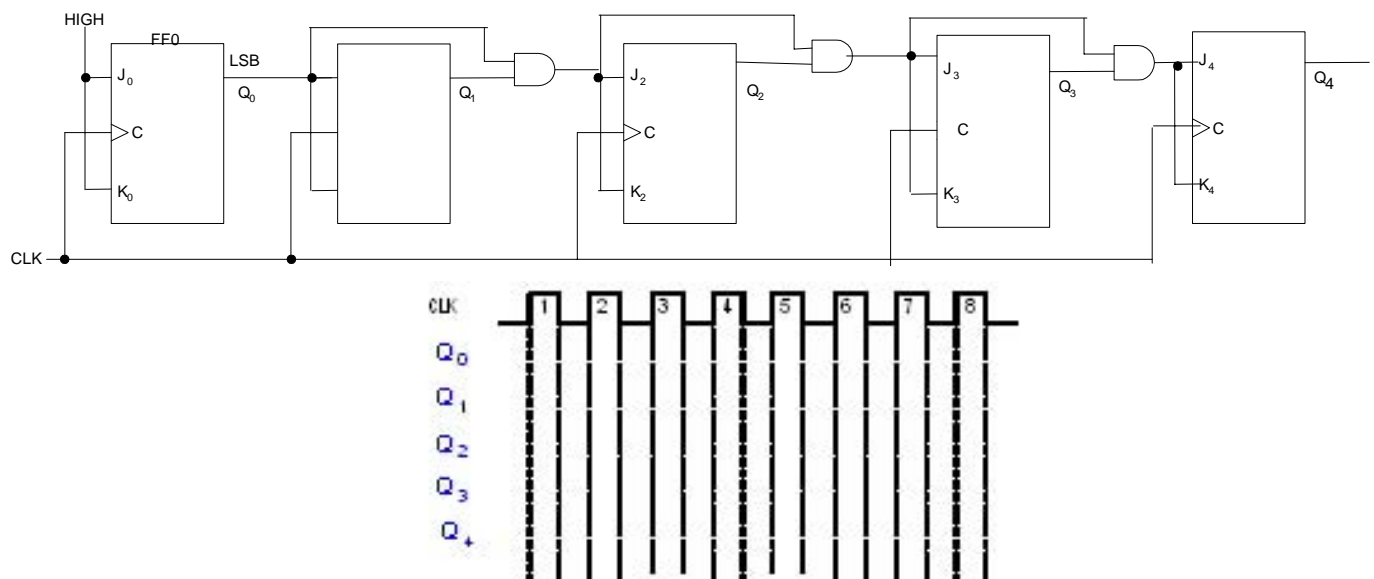




Question No: 3

Marks: 10

Show the complete timing diagram for the 5 stage synchronous binary counter.



Question No: 4

Marks: 10

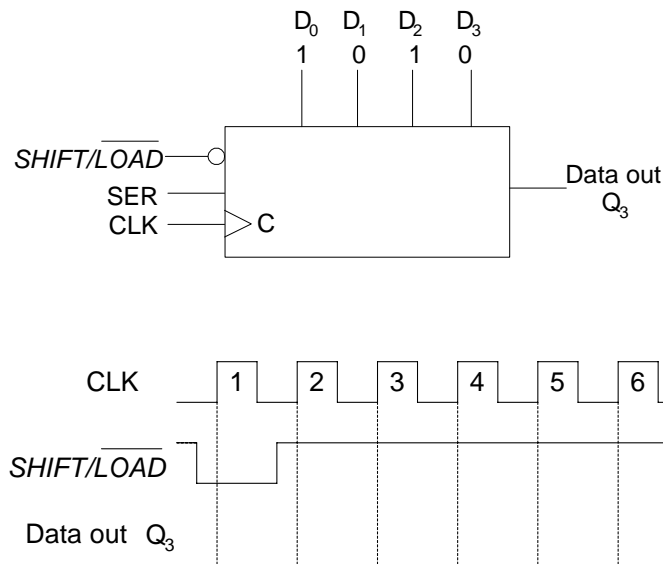
It is required to construct a memory with 256 words, 16 bits per word. Cores are available in a matrix of 16 rows and 16 columns.

- How many matrices are needed?
- How many flip-flops are in the address and buffer registers?
- How many cores receive current during a read cycle?
- How many cores receive at least half-current during a write cycle?

Question No: 5

Marks: 8

Show the data output waveform for a 4-bit register with the parallel input data and the clock and $\overline{SHIFT/LOAD}$ waveform given in the figure. The serial data input (SER) is a 0. The parallel data inputs are $D_0=1$, $D_1=0$, $D_2=1$, $D_3=0$ as shown. Develop the data-output waveform in relation to the inputs.



Question No: 6

Marks: 10

Implement a 4-bit Johnson Counter using J-K flip-flops

Question No: 7

Marks: 8

Briefly answer the following questions:

- What does sampling mean?
- Why you must hold a sampled value?
- If the highest frequency component in an analog signal is 20kHz, what is minimum sample frequency?
- What determines the accuracy of quantization process?