



MIDTERM EXAMINATION
SEMESTER SPRING 2005
CS302-Digital Logic Design (S1)

Total Marks:100
Duration:120 Min

Student ID / Login ID	
Name	
PVC Name / Code	
Date	

Maximum Time Allowed: (2 Hours)

Please read the following instructions carefully before attempting any of the questions:

1. Attempt all questions.
2. Calculators are **NOT** allowed.
3. Do not ask any questions about the contents of this examination from anyone.
 - a. If you think that there is something wrong with any of the questions, attempt it to the best of your understanding.
 - b. If you believe that some essential piece of information is missing, make an appropriate assumption and use it to solve the problem.
4. **Circuit Diagrams, Equations and Truth Tables** should be clear.

Write down all the steps in Subjective Questions. Marks will be deducted for missing steps.

****WARNING: Please note that Virtual University takes serious note of unfair means. Anyone found involved in cheating will get an `F` grade in this course.**

For Teacher's use only									
Question	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Total
Marks									

Question No: 1

Marks: 2+2+2+2+2=10

Select the best possible choice.

- 1) The OR gate performs Boolean _____.
 - a) multiplication
 - b) subtraction
 - c) division
 - d) addition

- 2) How many states does a modulus-4 counter have?
 - a) 1
 - b) 2
 - c) 4
 - d) 16

- 3) How will a serial in/serial out shift register accept data serially?
 - a) one bit at a time
 - b) 8 bits at a time
 - c) only after a load pulse
 - d) only after being cleared

- 4) The invalid state of an SR latch occurs when
 - a) S=1,R=0
 - b) S=0,R=1
 - c) S=1,R=1
 - d) S=0,R=0

- 5) The storage cell in SRAM is
 - a) a flip -flop
 - b) a capacitor
 - c) a fuse

d) a magnetic domain

Question No: 2

Marks: 12+2+2=16

a) Simplify the Boolean function using k-map and draw the circuit diagram.

$$F(x, y, z) = \sum (1, 3, 5, 6, 7)$$

b) Define JEDEC file

c) What is 2's complement of 0011 1001?

Question No: 3

Marks: 10

Draw the circuit diagram of the 4x1 Multiplexer. Also write down its truth table?

Question No: 4

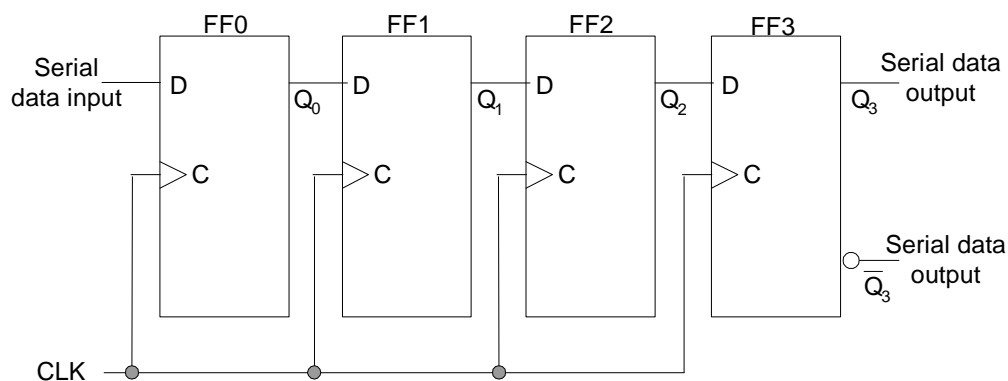
Marks: 20

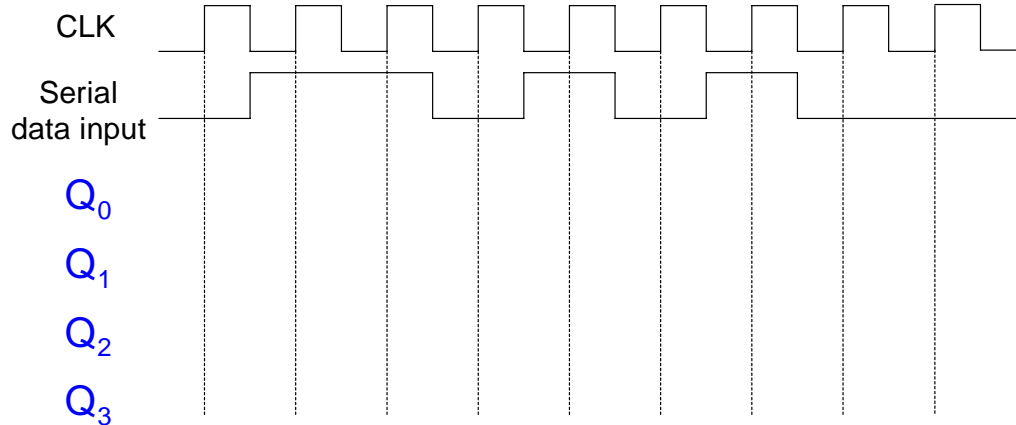
Design a 2-bit count-down counter. This is a sequential circuit with two flip flops and one input x. when x=0 the state of flip flop doesn't change. When x=1 the state sequence is 11, 10, 01, 00, 11 and repeat.

Question No: 5

Marks: 12

For the data input and clock in figure, determine the states of each flip-flop in the shift register for the diagram and show the Q waveforms. Assume that the register contains all 1s initially.





Question No: 6

Marks: 12

Draw block diagram of 4-bit Johnson Counter?

Question No: 7

Marks: 6+4

- a) Answer the following questions briefly:
 - a. What is current sourcing?
 - b. Define noise margin?
- b) Name any four performance characteristics of Digital-to-Analog Converters.

Question No: 8

Marks: 2+2+1+5=10

- a) What does DSP stands for?
- b) What does SIMM stands for?
- c) Define ROM and list the types of read-only memories?